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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,581	ADAMS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21, 22, 24, 25, 26, 27, 28, 30, 31, 32, 33, 35, 36, 37, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,513,089 to Hofmann et al. ("Hofmann"), Applicant Admitted Prior Art ("AAPA"), and US Patent Number 6,209,118 to LaBerge ("LaBerge").

3. In reference to Claim 21, Hofmann teaches a processor core physically located upon a single integrated circuit (See Figure 1 'PPC405 CPU'); one or more peripherals physically located upon said integrated circuit (See Figure 1 'I^2C', 'GPIO', 'UART', and 'DMA Controller'); and coupling a first internal bus to said processor core and to said peripheral(s) (See Figure 1 Number 101), said first internal bus carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said coupling of said first internal bus further

comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit; and wherein adding said arbitrary number of pipeline stages to said first internal bus at floorplanning does not require a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 1, in order to enable shorter clock cycles by

reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

4. In reference to Claim 22, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 21 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1 'DMA Controller'), providing a memory subsystem physically located upon said single integrated circuit (See Figure 1 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller' and Figure 2 'On-Chip Memory'); and coupling a second internal bus physically located upon said single integrated circuit to said processor core, to said memory subsystem, and to said DMA-type peripherals (See Figure 1 Number 102). Hofmann does not teach that said second internal bus has a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said coupling of said second internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit; and wherein adding said arbitrary number of pipeline stages to said second internal bus at floorplanning does not require a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target

(See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 22, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

5. In reference to Claim 24, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 21 and 22 above. AAPA further teaches that a common solution in creating a pipeline is to insert a flip-flop in the path to capture and re-launch the signal (See Page 4 Lines 15-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 24, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

6. In reference to Claim 25, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 22 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both busses to access a plurality of common devices (See Figure 1), and that each topology is a bussed topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline

segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 25, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

7. In reference to Claim 26, Hofmann teaches initiating and receiving signals using a processor core physically located upon a single integrated circuit (See Figure 1 'PPC405 CPU'); initiating and receiving signals using one or more peripherals physically located upon said single integrated circuit (See Figure 1 'I^2C', 'GPIO', 'UART', and 'DMA Controller'); and carrying signals from signal initiators to signal targets using a first internal bus physically located upon said single integrated circuit coupled to said processor core and to said peripheral(s) (See Figure 1 Number 101) Hofmann does not teach that said first internal bus has a latency tolerant signal protocol; wherein said first internal bus further comprises an arbitrary number of pipeline stages, wherein one or more of said arbitrary number of pipeline stages has been added between any signal initiator and any signal target when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of

pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 26, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

8. In reference to Claim 27, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 26 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and said method further comprises: initiating and receiving signals using a memory subsystem physically located upon said single integrated circuit (See Figure 1 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller' and Figure 2 'On-Chip Memory'); and carrying signals from signal initiators to signal targets using a second internal bus physically located upon said single integrated circuit coupled to said processor core, to said memory subsystem, and to said DMA-type peripherals (See Figure 1 Number 102). Hofmann does not teach that said second internal bus has a latency tolerant signal protocol; wherein said second internal bus further comprises an arbitrary number of pipeline stages, wherein one or more of said arbitrary number of pipeline stages has been added between any signal initiator and any signal target when floorplanning said single integrated circuit; and wherein adding said one or more of said arbitrary number of pipeline stages to said second internal bus at floorplanning does not require a subsequent design change. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12

and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 27, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

9. In reference to Claim 29, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 26 and 26 above. AAPA further teaches that a common solution in

creating a pipeline is to insert a flip-flop in the path to capture and re-launch the signal (See Page 4 Lines 15-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 29, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

10. In reference to Claim 30, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 27 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both busses to access a plurality of common devices (See Figure 1), and that each topology is a bussed topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by

LaBerge, resulting in the invention of Claim 30, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

11. In reference to Claim 31, Hofmann teaches a processor core physically located upon a single integrated circuit (See Figure 1 'PPC405 CPU'); one or more peripherals physically located upon said integrated circuit (See Figure 1 'I^2C', 'GPIO', 'UART', and 'DMA Controller'); and a first internal bus physically located upon said single integrated circuit coupled to said processor core and to said peripheral(s) (See Figure 1 Number 101), said first internal bus carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said first internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target, one or more of said arbitrary number of pipeline stages having been added when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal

bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 31, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

12. In reference to Claim 32, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 31 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1 'DMA Controller'), providing a memory subsystem physically located upon said single integrated circuit (See Figure 1 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller' and Figure 2 'On-Chip Memory'); and a second internal bus physically located upon said single integrated circuit coupled to said processor core, to said memory subsystem, and to said DMA-type peripherals (See Figure 1 Number 102). Hofmann does not teach that said second internal bus has a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said first internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target, one or more of said arbitrary number of pipeline stages having been added when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and

Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 32, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

13. In reference to Claim 34, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 31 and 32 above. AAPA further teaches that a common solution in creating a pipeline is to insert a flip-flop in the path to capture and re-launch the signal (See Page 4 Lines 15-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline

segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 34, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

14. In reference to Claim 35, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 32 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both busses to access a plurality of common devices (See Figure 1), and that each topology is a bussed topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 35, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that

they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

15. In reference to Claim 36, Hofmann teaches a processor core physically located upon a single integrated circuit (See Figure 1 'PPC405 CPU'); one or more peripherals physically located upon said integrated circuit (See Figure 1 'I^2C', 'GPIO', 'UART', and 'DMA Controller'); and a first internal bus physically located upon said single integrated circuit coupled to said processor core and to said peripheral(s) (See Figure 1 Number 101), said first internal bus carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said first internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target, one or more of said arbitrary number of pipeline stages having been added when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing

programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 36, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

16. In reference to Claim 37, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 36 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1 'DMA Controller'), providing a memory subsystem physically located upon said single integrated circuit (See Figure 1 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller' and Figure 2

'On-Chip Memory'); and a second internal bus physically located upon said single integrated circuit coupled to said processor core, to said memory subsystem, and to said DMA-type peripherals (See Figure 1 Number 102). Hofmann does not teach that said second internal bus has a latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said first internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target, one or more of said arbitrary number of pipeline stages having been added when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration. AAPA teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target (See Page 4 Lines 15-23 and Page 6 Line 19 – Page 7 Line 2); and wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit (See Page 5 Lines 9-12 and Page 6 Line 19 – Page 7 Line 2). LaBerge teaches a system controller ASIC, which is equivalent to a SOC (See Figure 1 Number 30), containing programmable circuits, which are equivalent to the pipeline stages (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into a chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and Lines 30-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 37, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

17. In reference to Claim 39, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 36 and 37 above. AAPA further teaches that a common solution in creating a pipeline is to insert a flip-flop in the path to capture and re-launch the signal (See Page 4 Lines 15-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 39, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit

designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

18. In reference to Claim 40, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claim 36 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both busses to access a plurality of common devices (See Figure 1), and that each topology is a bussed topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, resulting in the invention of Claim 40, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA) and to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge).

19. Claims 23, 28, 33, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann, AAPA, and LaBerge as applied to Claims 21, 22, 26, 27,

31, 32, 36, and 37 above, and further in view of US Patent Numbers 6,493,407 to Sheafor et al. ("Sheafor"), US Patent Number 6,173,349 to Qureshi et al. ("Qureshi"), and US Patent Number 5,469,547 to Pawlowski et al. ("Pawlowski").

20. In reference to Claim 23, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 21 and 22 above. Hofmann, AAPA, and LaBerge do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann, AAPA, and LaBerge with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 23, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of

information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

21. In reference to Claim 28, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 26 and 27 above. Hofmann, AAPA, and LaBerge do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann, AAPA, and LaBerge with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 28, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

22. In reference to Claim 33, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 31 and 32 above. Hofmann, AAPA, and LaBerge do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann, AAPA, and LaBerge with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 33, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

23. In reference to Claim 38, Hofmann, AAPA, and LaBerge teach the limitations as applied to Claims 36 and 37 above. Hofmann, AAPA, and LaBerge do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann, AAPA, and LaBerge with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 38, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

Drawings

24. Figures 1A, 1B, and 1C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

25. Applicant's arguments with respect to Claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. Applicant has cancelled Claims 1-20 and added new claims 21-40 having a substantially different scope.

Conclusion

26. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US Patent Number 4,584,653 to Chih et al.; US Patent

Number 6,321,371 to Yount, Jr.; US Patent Number 6,594,814 to Jou et al.; and US Patent Application Publication Number 2002/0199085 to Norden et al.

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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